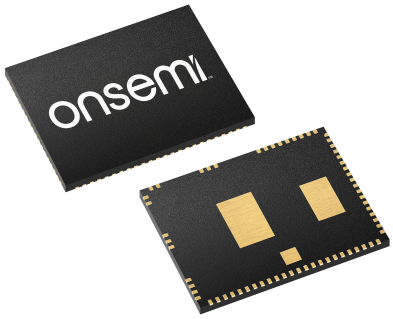
Sensorless BLDC ecoSpin Motor Controller, with Gate Drivers

Arm® Cortex®–M0+, 600 V, FAN73896

ECS640A



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Overview

EcoSpin Motor Controller ECS640A is a 3–phase BLDC configurable motor control system in package that integrates an ultra–low–power optimized Arm Cortex–M0+ microcontroller (Nebo–40–64), three sense amplifiers and a reference amplifier (NCS20034), three bootstrap diodes, and a high–voltage gate–driver designed for high–voltage, high–speed operation, with the ability to drive MOSFETs and IGBTs operating up to 600 V (FAN73896). Six gate driver outputs provide sink/source of 350 mA/650 mA (typ) gate current to external power devices. The device includes Hall Sensor inputs to support either sensored or sensorless operation. Three independent low–side source pins allow for single or multiple shunt measurement.

Protection functions include under–voltage lockout and inverter over–current trip with an automatic fault–clear function. An open–drain fault signal is provided to indicate that a fault condition has occurred.

Direct Torque & Flux Control (DTFC) firmware is available and allows optimal motor performance on the Arm Cortex–M0+ platform.

The small footprint and integration make this device a perfect fit with discrete power devices to maximize scalability across platforms and to minimize area requirements as power levels scale.

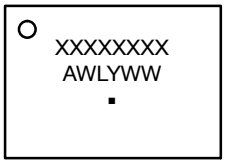
Features

- Arm Cortex–M0+ (Nebo–40–64)
  - 40 MHz Clock Frequency
  - 8 kB RAM Memory
  - 64 kB Flash Memory
- 600 V Gate Driver (FAN73896)
  - 350 mA/650 mA Sourcing/Sinking Current Driving Capability
- 4 Sense Amps for Current Sensing (NCS20034)
- Integrated Bootstrap Diodes
- Communication: I^2C, UART and SPI
- Firmware Available, Sensorless Direct Torque and Flux Control
- Max Power Dissipation: 1.8 W
- Temperature Range: –40 to 105°C
- These are Pb–Free Devices

Typical Applications

- Three–Phase Brushless DC (BLDC) Sensorless Motor Control
- Three–Phase Brushless DC (BLDC) Sensor Based Motor Control

MARKING DIAGRAM



XXXXXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
▪	= Logo(s)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

End Products

- HVAC
- Home Appliances: Refrigerators, Fabric Care, Dishwashers
- Pumps
- General Purpose Three–Phase Motor Control

Safety Mechanisms Highlight

- Over–Current Shutdown Turns Off All Six Channels

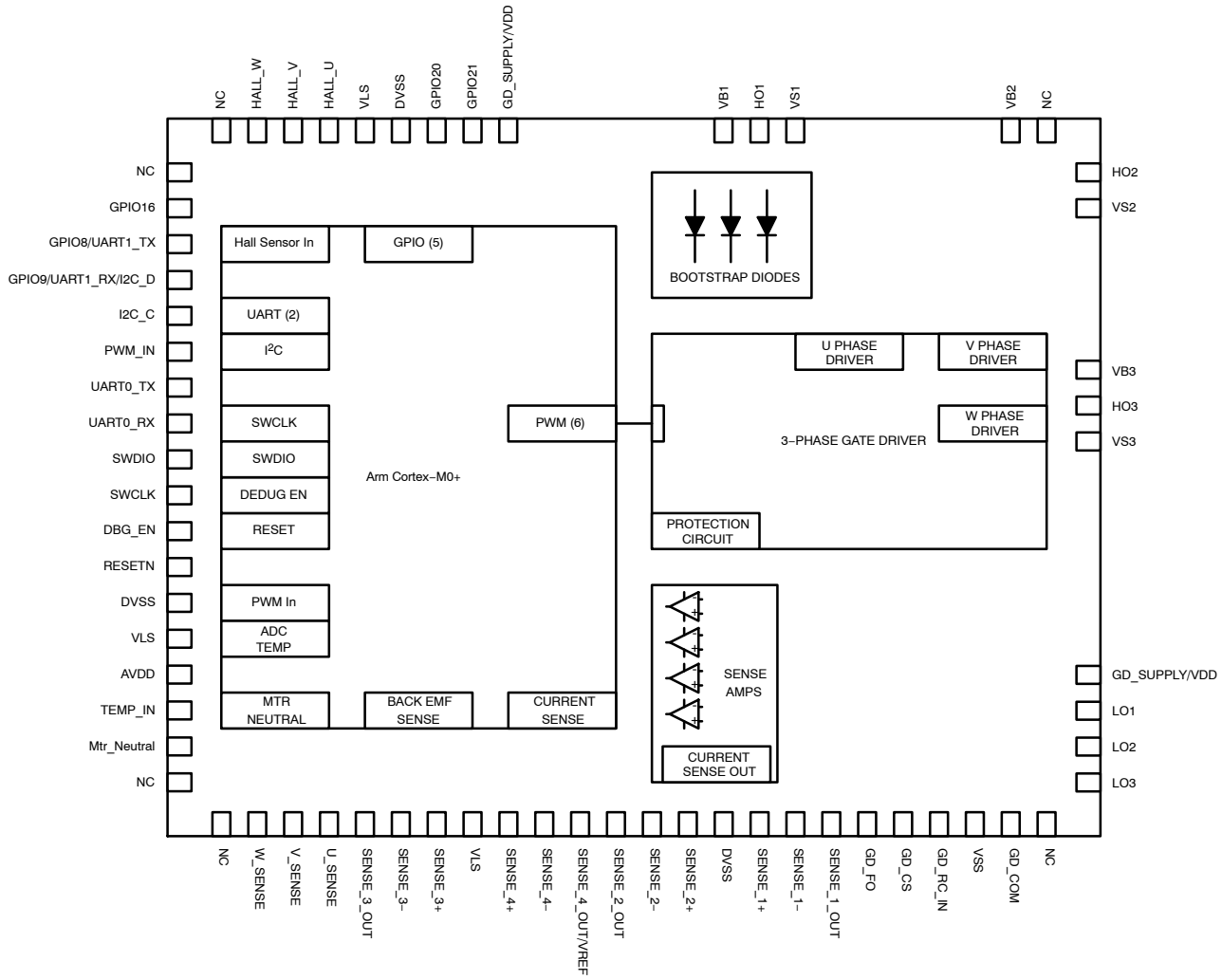


Figure 1. Block Diagram

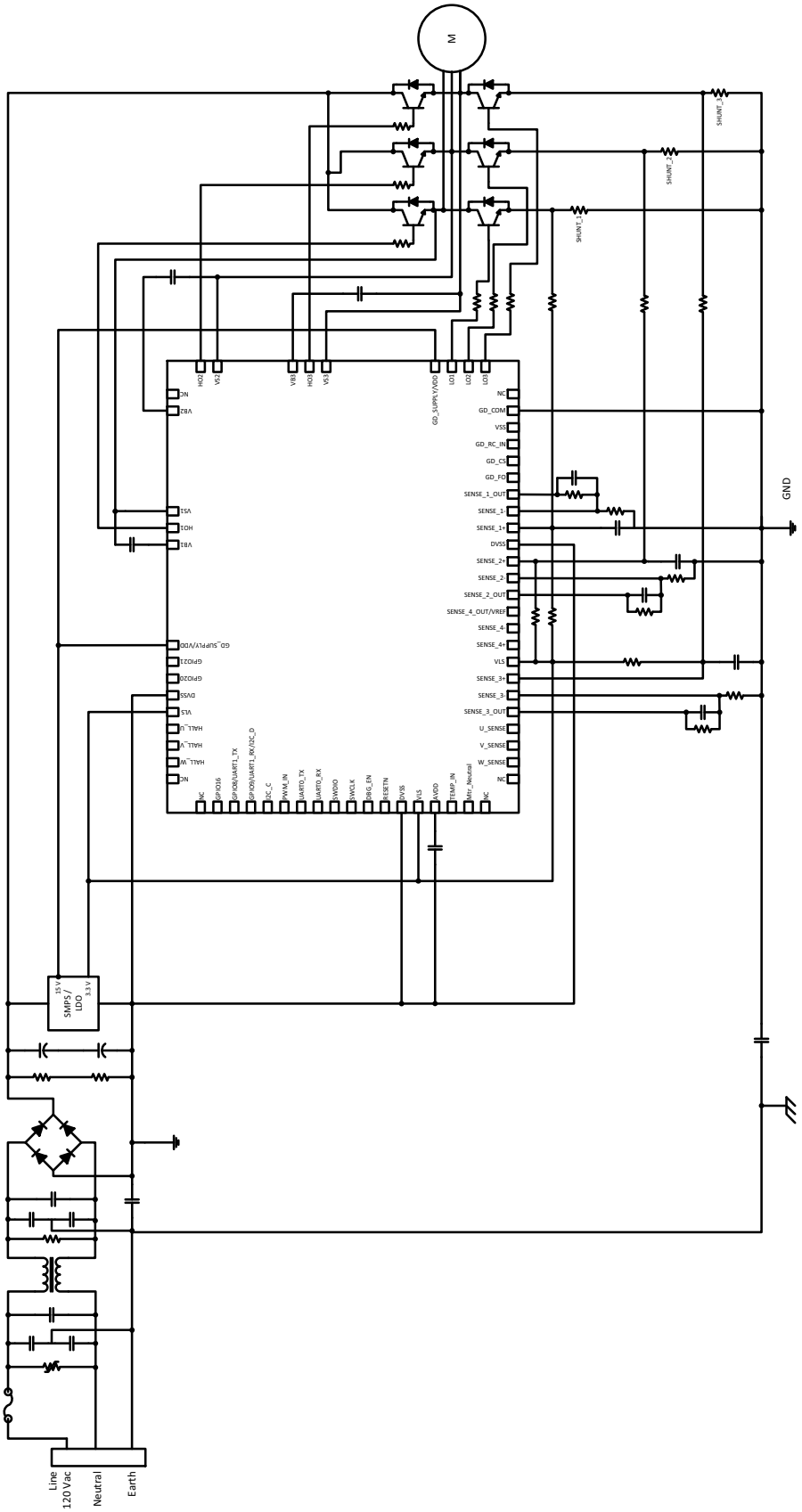


Figure 2. Application Schematic

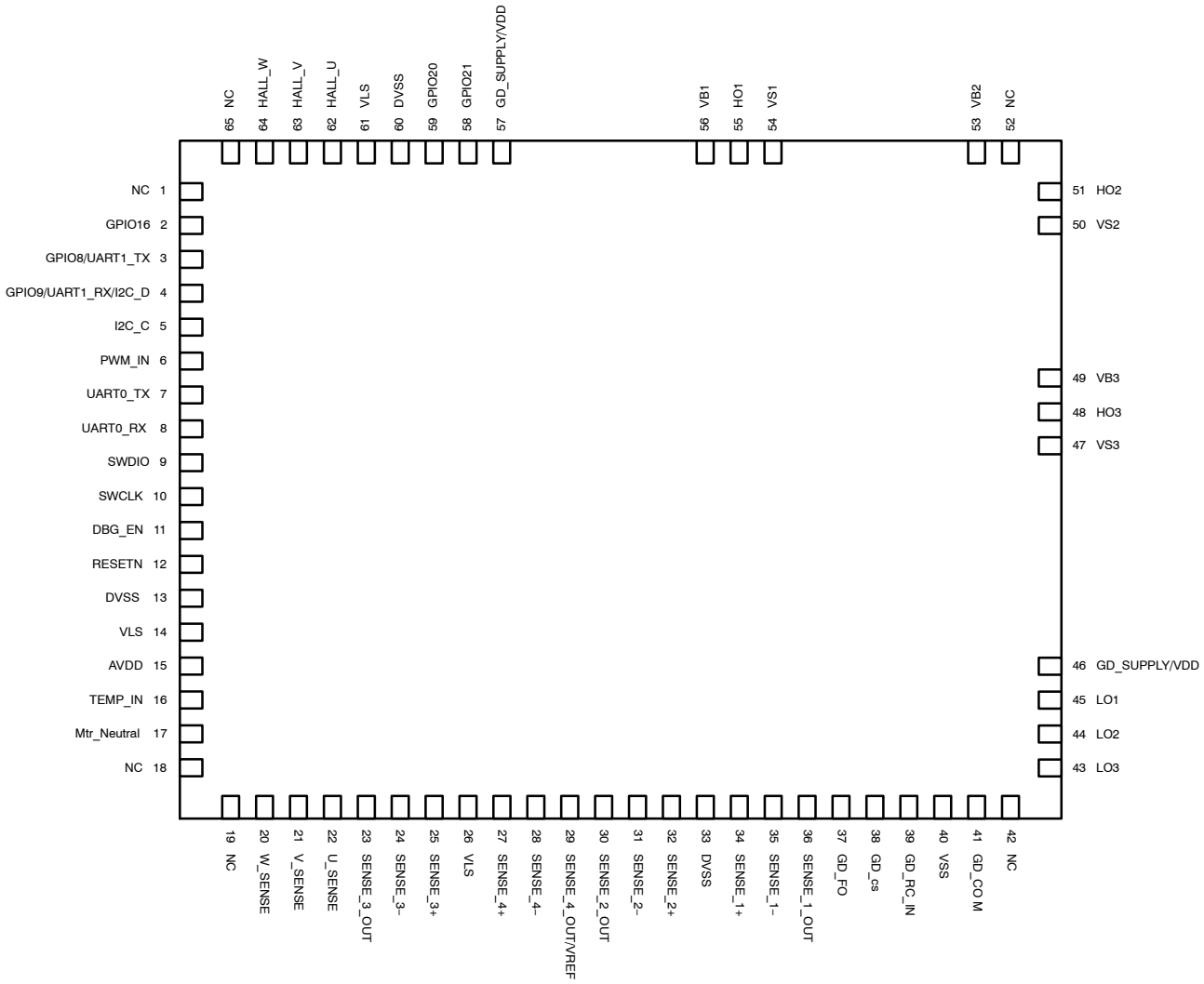


Figure 3. Pin Connections

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Description
1	NC	–
2	GPIO16	General Purpose IO (Nebo40−64 PC0 I/O)
3	GPIO8 / UART1_TX	General Purpose IO / UART Transmit (Nebo40−64 PB0 I/O)
4	GPIO9 / UART1_RX / I2C_D	General Purpose IO / UART Receive / I^2C (Nebo40−64 PB1 I/O)
5	I2C_C	I2C (Nebo40−64 PB2 I/O)
6	PWM_IN	PWM Input Signal (Nebo40−64 PB3 I/O)
7	UART0_TX	UART Transmit (Nebo40−64 PB4 I/O)
8	UART0_RX	UART Receive (Nebo40−64 PB5 I/O)
9	SWDIO	Single Wire Interface Data (Nebo40−64 PB6 I/O)
10	SWCLK	Single Wire Interface Clock (Nebo40−64 PB7 I/O)
11	DBG_EN	Debug Enable (Nebo40−64 DBG_EN)
12	RESETN	μC Reset (Nebo40−64 RESETN)
13	DVSS	Ground
14	VLS	3.3 V Supply for Micro−Controller

PIN FUNCTION DESCRIPTION (continued)

Pin #	Pin Name	Description
15	AVDD	Analog Reference Voltage Out
16	TEMP_IN / GP_A_1	General Analog Input or Temperature Sensor Input (Nebo40−64 PA0 I/O)
17	Mtr_Neutral / GP_A_0	Motor Center Tap Input or Bus Voltage Input (Nebo40−64 PA1 I/O)
18	NC	−
19	NC	−
20	W_SENSE	Back EMF Sense Pin − Phase W (requires reduction and filtering) (Nebo40−64 PA2 I/O)
21	V_SENSE	Back EMF Sense Pin − Phase V (requires reduction and filtering) (Nebo40−64 PA3 I/O)
22	U_SENSE	Back EMF Sense Pin − Phase U (requires reduction and filtering) (Nebo40−64 PA4 I/O)
23	SENSE_3_OUT	Amplifier 3 Output (Nebo40−64 PA5 I/O)
24	SENSE_3−	Amplifier 3−
25	SENSE_3+	Amplifier 3+
26	VLS	3.3 V Supply for Amplifier
27	SENSE_4+	Amplifier 4+
28	SENSE_4−	Amplifier 4−
29	SENSE_4_OUT / VREF	Sense Amplifier can be used for voltage reference
30	SENSE_2_OUT	Amplifier 2 Output (Nebo40−64 PA7 I/O)
31	SENSE_2−	Amplifier 2+
32	SENSE_2+	Amplifier 2−
33	DVSS	Amplifier V_{SS}
34	SENSE_1+	Amplifier 1+
35	SENSE_1−	Amplifier 1−
36	SENSE_1_OUT	Amplifier 1 Output (Nebo40−64 PA6 I/O)
37	GD_FO	Fault output (Nebo40−64 PC6 I/O) (FAN73896 FO output)
38	GD_CS	Analog input for over−current shutdown (FAN73896 CS input)
39	GD_RC_IN	External RC network input used to define the fault−clear delay
40	VSS	Gate Driver V_{SS}
41	GD_COM	Gate Driver Low Side Common
42	NC	−
43	LO3	Low−Side Gate Driver 3 Output
44	LO2	Low−Side Gate Driver 2 Output
45	LO1	Low−Side Gate Driver 1 Output
46	GD_Supply / VDD	15 V supply for Gate Driver
47	VS3	High−Side Driver 3 Floating Supply Offset Voltage
48	HO3	High−Side Driver 3 Gate Driver Output
49	VB3	High−Side Supply 3 Floating Supply
50	VS2	High−Side Driver 2 Floating Supply Offset Voltage
51	HO2	High−Side Driver 2 Gate Driver Output
52	NC	−
53	VB2	High−Side Driver 2 Floating Supply
54	VS1	High−Side Driver 1 Floating Supply Offset Voltage
55	HO1	High−Side Driver 1 Gate Driver Output
56	VB1	High−Side Driver 1 Floating Supply
57	GD_Supply / VDD	15 V Supply for Gate Driver

PIN FUNCTION DESCRIPTION (continued)

Pin #	Pin Name	Description
58	GPIO21	General Purpose IO (Nebo40−64 PC5 I/O)
59	GPIO20	General Purpose IO (Nebo40−64 PC4 I/O)
60	DVSS	Ground
61	VLS	3.3 V Supply for Micro−Controller
62	HALL_U	Hall Sensor Input U (Nebo40−64 PC3 I/O)
63	HALL_V	Hall Sensor Input V (Nebo40−64 PC2 I/O)
64	HALL_W	Hall Sensor Input W (Nebo40−64 PC1 I/O)
65	NC	−
Exposed Thermal Pads		See recommended mounting footprint.

MAXIMUM RATINGS

Rating	Symbol	Minimum	Maximum	Unit
Primary Supply Voltage − MCU	V_{LS}	−0.3	3.6	V
Ground Voltage	DV_{SS}	−0.3	−	V
Input Voltage Range (Note 1)	V_{IN}	DV_{SS} − 0.3	V_{DD} + 0.3	V
Input Pin Current − MCU	I_{IN}	−10	10	mA
Power Dissipation	P_D	−	1.8	W
Ambient Temperature	T_A	−40	105	°C
Storage Temperature Range	T_{STG}	−55	150	°C
GATE DRIVER				
High−Side Floating Offset Voltage	V_S	$V_{B1,2,3}$ − 25	$V_{B1,2,3}$ + 0.3	V
High−Side Floating Supply Voltage	V_B	−0.3	625.0	V
Low−Side and Logic−Fixed Supply Voltage	V_{DD}	−0.3	25.0	V
High−Side Floating Output Voltage $V_{HO1,2,3}$	V_{HO}	$V_{S1,2,3}$ − 25	$V_{S1,2,3}$ + 0.3	V
Low−Side Floating Output Voltage $V_{LO1,2,3}$	V_{LO}	−0.3	V_{DD} + 0.3	V
Input Voltage	V_{IN}	−0.3	5.5	V
Fault Output Voltage (FO)	V_{FO}	−0.3	V_{DD} + 0.3	V
High−Side Input Pulse Width	PW_{HIN}	500	−	Ns
Allowable Offset Voltage Slew Rate	dV_s/dt	−	±50	V/ns
BOOTSTRAP DIODE				
Maximum Repetitive Reverse Voltage	V_{RRM}	−	600	V
Forward Current	I_F	−	0.50	A
Forward Current (Peak)	I_{FP}	−	1.50	A
CURRENT SENSOR AMPLIFIER				
Supply Voltage (V_{DD} − V_{SS})	V_{DD} (Pin33)	−0.3	3.6	V
ESD Capability, Human Body Model (Note 2)	V_{HBM}	−	≥2000	V
ESD Capability, Charged Device Model (Note 2)	V_{CDM}	−	≥1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78

THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Resistance – Junction to Ambient (Note 4)	Θ_{JA}	24.6	°C/W
Thermal Resistance – Junction to Case	Θ_{JC}	4.9	°C/W

3. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Supply Voltage	V_{LS}	3.0	3.6	V
Ambient Temperature	T_A	−40	85	°C
GATE DRIVER				
High−Side Floating Supply Voltage	$V_{B1,2,3}$	$V_{s1,2,3}$ + 10	$V_{s1,2,3}$ + 20	V
High−Side Floating Supply Offset Voltage	$V_{s1,2,3}$	6 – V_{DD}	600	V
Low−Side and Logic Fixed Supply Voltage	V_{DD}	12	20	V
High−Side Output Voltage	$V_{HO1,2,3}$	$V_{s1,2,3}$	$V_{B1,2,3}$	V
Low−Side Output Voltage	$V_{LO1,2,3}$	COM	V_{DD}	V
Fault Output Voltage (FO)	V_{FO}	V_{SS}	V_{DD}	V
Current−Sense Pin Input Voltage	V_{CS}	V_{SS}	5	V
Logic Input Voltage (HIN1,2,3 and LIN1,2,3)	V_{IN}	V_{SS}	5	V
Low−Side Driver Return	COM	−5	5	V
BOOTSTRAP DIODE				
Forward Voltage	V_F	–	–	V
Reverse−Recovery Time	t_{rr}	–	–	ns
CURRENT SENSOR AMPLIFIER				
Operating Supply Voltage (V_{DD} – V_{SS})	V_s	1.8	3.6	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
$MCUV_{DDIO}$ = 3.3 V, T_A = 30°C						
Digital I/O						
Logic Input Low Threshold		V_{IL}	0.3	–	–	V_{DD}
Logic Input High Threshold		V_{IH}	–	–	0.7	V_{DD}
Internal Pull−up Resistor		R_{PU}	35	–	–	kΩ
Internal Pull−down Resistor		R_{PD}	35	–	–	kΩ
Logic Output Low Level	I_{LOAD} = 4 mA at V_{DDIO} = 1.8 V	V_{OL}	–	–	0.5	V
Logic Output High Level	I_{LOAD} = 4 mA at V_{DDIO} = 1.8 V	V_{OH}	V_{DD} – 0.5	–	–	V
Pin Leakage		I_{LEAK}	−1	–	1	μA
Flash Memory						
Read Access Time		T_{ACC}	–	–	40	ns
Program Time		T_{PROG}	–	–	20	μs
Page/Mass Erase Time		T_{ERASE}	–	–	10	ms
Data Retention		T_{RET}	10	–	–	Years

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Flash Memory						
Flash Endurance Erase Cycles	at 25°C		100k	–	–	Cycles
	at 85°C		10k	–	–	
Power−On RESET and BROWN−OUT						
Power−on Voltage Trip Point	Rising	V_{POR_R}	1.540	–	1.635	V
	Falling	V_{POR_F}	1.455	–	1.635	
Brownout Trip Point	Rising	V_{BO_R}	1.525	–	1.71	V
	Falling	V_{BO_F}	1.5	–	1.685	
High Speed RC Oscillator (HSOSC)						
Oscillator Frequency	40 MHz	F_{HSOSC}	38.80	40.00	41.20	MHz
Temperature Drift	Temp Co = +3% Cold and −3% Hot	ΔF_{HSOSC}	–	±3%	–	
Oscillator Start−up Time		T_{HSOSC_SU}	–	2	–	μs
Current Consumption		I_{HSOSC}	–	350	–	μA
Low Power RC Oscillator (LPOSC)						
Oscillator Frequency (Fast Mode)	Trimmed	F_{LPOSC}	–	10.24	–	kHz
Oscillator Frequency (Slow Mode)	Trimmed	F_{LPOSC}		640	–	Hz
Temperature Drift		ΔF_{LPOSC}	–	±6%	–	
Oscillator Start−up Time (Fast Mode)		T_{LPOSC_SU}	–	0.41	–	ms
Oscillator Start−up Time (Slow Mode)		T_{LPOSC_SU}	–	1.4	–	ms
Current Consumption (Fast Mode)		I_{LPOSC}	–	420	–	nA
Current Consumption (Slow Mode)		I_{LPOSC}	–	95	–	nA
High Speed Crystal Oscillator						
Crystal Frequency		F_{HSXTAL}	8	32	40	MHz
Low Power Crystal Oscillator						
Crystal Frequency		F_{LPXTAL}	–	32.768	–	kHz
Current Consumption		I_{LPXTAL}	–	285	–	nA
Analog Comparators						
Common Mode Input Range		V_{CMIR}	0.2	–	V_{DDIO} − 0.5	V
Response Time		T_{COMP}	–	200	–	ns
Analog to Digital Converter (ADC)						
Sample Clock Frequency		F_{ADCCLK}	0.01	–	20	MHz
−0.5dBFS Power Bandwidth		F_{BW}	50	–	–	kHz
Input Capacitance (when 1:1 divider is selected (single−ended)) (Note 5)		C_{IN}	–	2	–	pF
Gain Error (Note 6)		E_{GAIN}	–	±0.75	–	%
Offset Error (Note 6)		E_{OFFSET}	–	±15	–	LSB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Analog to Digital Converter (ADC)						
Integral Non−Linearity (Note 7)	Differential, gain bypass, 1 V reference	INL	−2.5	−	2.5	LSB
	Differential, 1X gain, 1 V reference		−	±2.5	−	
	Differential, 10X gain, 1 V reference		−	±3.5	−	
	Differential, 1/4 gain, 1 V reference		−	±2	−	
	Single−ended, 1X gain, 1 V reference, 2X V_{ref} Range (Note x6)		−	±2	−	
Differential Non−Linearity (Note 7)	Differential, gain bypass, 1 V reference	DNL	−	−	1.5	LSB
	Differential, 1X gain, 1 V reference		−	1.5	−	
	Differential, 10X gain, 1 V reference		−	2.0	−	
	Differential, 1/4 gain, 1 V reference		−	1.5	−	
	Single−ended, 1X gain, 1 V reference, 2X V_{ref} Range (Note x6)		−	1.5	−	
GATE DRIVER						
Low−Side Power Supply Section						
Quiescent V_{DD} Supply Current	$V_{LIN1,2,3}$ = 0 V or 5 V, EN = 0 V	I_{QDD}	−	250	400	μA
Operating V_{DD} Supply Current	C_{LOAD} = 1 Nf, $f_{LIN1,2,3}$ = 20 kHz, rms Value	I_{PDD}	−	550	750	μA
V_{DD} Supply Under−Voltage Positive−Going Threshold	V_{DD} = Sweep	V_{DDUV+}	9.7	11.0	12.0	V
V_{DD} Supply Under−Voltage Negative−Going Threshold	V_{DD} = Sweep	$V_{DDUV−}$	9.2	10.5	11.4	V
V_{DD} Supply Under−Voltage Lockout Hysteresis	V_{DD} = Sweep	V_{DDHYS}	−	0.5	−	V
Bootstrapped Power Supply Section						
V_{BS} Supply Under−Voltage Positive−Going Threshold	$V_{BS1,2,3}$ = Sweep	V_{BSUV+}	9.7	11.0	12.0	V
V_{BS} Supply Under−Voltage Negative−Going Threshold	$V_{BS1,2,3}$ = Sweep	$V_{BSUV−}$	9.2	10.5	11.4	V
V_{BS} Supply Under−Voltage Lockout Hysteresis	$V_{BS1,2,3}$ = Sweep	V_{BSHYS}	−	0.5	−	V
Offset Supply Leakage Current	$V_{S1,2,3}$ = $V_{S1,2,3}$ = 600 V	I_{LK}	−	−	10	μA
Quiescent V_{BS} Supply Current	$V_{HIN1,2,3}$ = 0 V or 5 V, EN = 0 V	I_{QBS}	10	50	80	μA
Operating V_{BS} Supply Current	C_{LOAD} = 1 nF, $f_{HIN1,2,3}$ = 20 kHz, rms Value	I_{PBS}	200	320	480	μA
Gate Driver Output Section						
High−Level Output Voltage, V_{BIAS} − V_O	I_O = 0 mA (No Load)	V_{OH}	−	−	100	MV
Low − Level Output Voltage, V_O	I_O = 0 mA (No Load)	V_{OL}	−	−	100	mV
Output HIGH Short−Circuit Pulse Current	V_O = 15 V, V_{IN} = 0 V with PW ≤ 10 μs	I_{O+}	250	350	−	mA
Output LOW Short−Circuit Pulsed Current	V_O = 0 V, V_{IN} = 5 V with PW ≤ 10 μs	$I_{O−}$	500	650	−	mA
Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO		V_S	−	−9.8	−9.0	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Logic Input Section						
Logic “1” Input Voltage HIN1,2,3, LIN1,2,3		V_{IH}	2.5	–	–	V
Logic “0” Input Voltage HIN1,2,3, LIN1,2,3		V_{IL}	–	–	0.8	V
Logic Input Bias Current (HO = LO = HIGH)	V_{IN} = 5 V	I_{IN+}	77	100	143	μA
Logic Input Bias Current (HO = LO = LOW)	V_{IN} = 0 V	I_{IN-}	–	–	2	μA
Logic Input Pull−Up Resistance		R_{IN}	35	50	65	kΩ
Enable Control Section (EN)						
Enable Positive−Going Threshold Voltage		V_{EN+}	2.5	–	–	V
Enable Negative−Going Threshold Voltage		V_{EN-}	–	–	0.8	V
Logic Enable “1” Input Bias Current	V_{EN} = 5 V (Pull−Down = 150 kΩ)	I_{EN+}	15	33	50	μA
Logic Enable “0” Input Bias Current	V_{EN} = 0 V	I_{EN-}	–	–	2	μA
Logic Input Pull−Down Resistance		R_{EN}	100	150	333	kΩ
Over−Current Protection Section						
Over−Current Detect Positive Threshold		V_{CSTH+}	450	500	550	MV
Over−Current Detect Negative Threshold		V_{CSTH-}	–	440	–	mV
Over−Current Detect Hysteresis		V_{CSHYS}	–	60	–	mV
Short−Circuit Input Current	V_{CSIN} = 1 V	I_{CSIN}	5	10	15	μA
Soft Turn−Off Sink Current		I_{SOFT}	25	40	55	mA
Fault Output Section						
RCIN Positive−Going Threshold Voltage		$V_{RCINTH+}$	2.7	3.3	3.9	V
RCIN Negative−Going Threshold Voltage		$V_{RCINTH-}$	–	2.6	–	V
RCIN Hysteresis Voltage		$V_{RCINHYS}$	–	0.7	–	V
RCIN Internal Current Source	C_{RCIN} = 2 nF	I_{RCIN}	3	5	7	μA
Fault Output Low Level Voltage	V_{CS} = 1 V, I_{FO} = 1.5 mA	V_{FOL}	–	0.2	0.5	V
RCIN On Resistance	I_{RCIN} = 1.5 mA	R_{DSRCIN}	50	75	100	Ω
Fault Output On Resistance	I_{FO} = 1.5 mA	R_{DSFO}	90	130	170	Ω
Turn−On Propagation Delay	$V_{LIN1,2,3}$ = $V_{HIN1,2,3}$ = 5 V, $V_{S1,2,3}$ = 0 V	t_{ON}	350	500	650	ns
Turn−Off Propagation Delay	$V_{LIN1,2,3}$ = $V_{HIN1,2,3}$ = 0 V, $V_{S1,2,3}$ = 0 V	t_{OFF}	350	500	650	ns
Turn−On Rise Time	$V_{LIN1,2,3}$ = $V_{HIN1,2,3}$ = 5 V	t_R	20	50	100	ns
Turn−Off Fall Time	$V_{LIN1,2,3}$ = $V_{HIN1,2,3}$ = 0 V	t_F	10	30	80	ns
Enable LOW to Output Shutdown Delay		t_{EN}	400	500	600	ns
CS Pin Leading−Edge Blanking Time		t_{CSBLT}	400	650	850	ns
Time from CS Triggering to FO	From V_{CSC} = 1 V to FO Turn−Off	t_{CSFO}	–	850	1300	ns

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Fault Output Section						
Time from CS Triggering to Low−Side Gate Outputs Turn−Off	From V_{CSC} = 1 V to Starting Gate Turn−Off	t_{CSOFF}	−	850	1300	ns
Input Filtering Time (Note 7) (HINx, LINx, EN)		t_{FLTIN}	170	250	330	ns
Fault−Clear Time		t_{FLTCLR}	−	1.3	2.35	ns
Dead Time		DT	230	320	400	ns
Dead−Time Matching (All Six Channels) (Note 8)		MDT	−	−	50	ns
Delay Matching (All Six Channels) (Note 9)		MT	−	−	50	ns
Output Pulse−Width Matching (Note 10)	PW_{IN} > 1 μs	PM	−	50	100	ns
BOOTSTRAP DIODES						
Forward Voltage	I_F = 0.1 A, T_A = 25°C	V_F	−	2.5	−	V
Reverse−Recovery Time	I_F = 0.1 A, T_A = 25°C	t_{rr}	−	80	−	ns
CURRENT SENSOR AMPLIFIER (V_S = 1.8 V, T_A = +25°C)						
Input Characteristics						
Input Offset Voltage		V_{OS}	−	−	5.0	mV
Offset Voltage Drift		$\Delta V_{OS}/\Delta T$	−	2.0	6.0	μV/°C
Input Bias Current		I_{IB}	−	1	−	pA
Input Offset Current		I_{OS}	−	1	−	pA
Channel Separation		XTLK	−	100	−	dB
Input Resistance		R_{IN}	−	1	−	TΩ
Input Capacitance		C_{IN}	−	1.2	−	pF
Common Mode Rejection Ratio	V_{IN} = V_{SS} to V_{DD} − 0.6 V	CMRR	70	80	−	dB
	V_{IN} = V_{SS} + 0.2 V to V_{DD} − 0.6 V		65	−	−	
Output Characteristics						
Open Loop Voltage Gain	R_L = 10 kΩ	A_{VOL}	75	92	−	dB
	R_L = 2 kΩ		70	92	−	
Output Current Capability	Sourcing	I_{SC}	5	8	−	mA
	Sinking		10	14	−	
Output Voltage High	R_L = 10 kΩ	V_{OH}	1.75	1.798	−	V
	R_L = 2 kΩ		1.7	1.78	−	
Output Voltage Low	R_L = 10 kΩ	V_{OL}	−	7	100	mV
	R_L = 2 kΩ		−	20	100	
Noise Performance						
Voltage Noise Density	f = 1 kHz	e_N	−	20	−	nV/
Current Noise Density	f = 1 kHz	i_N	−	0.1	−	pA/
Dynamic Performance						
Gain Bandwidth Product		GBWP	−	5	−	MHz
Slew Rate at Unity Gain	Rising Edge, R_L = 2 kΩ, A_V = +1	SR	−	6	−	V/μs
	Falling Edge, R_L = 2 kΩ, A_V = +1		−	9	−	
Phase Margin	R_L = 10 kΩ, C_L = 5 pF	Ψ_m	−	53	−	°
Gain Margin	R_L = 10 kΩ, C_L = 5 pF	A_m	−	8	−	dB
Settling Time	V_O = 1 V_{pp}, Gain = 1, C_L = 20 pF, Settling time to 0.1%	t_s	−	1.8	−	μs

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Dynamic Performance						
Total Harmonics Distortion + Noise	V_O = 1 V_{pp}, R_L = 2 kΩ, A_V = +1, f = 1 kHz	THD+N	–	0.005	–	%
	V_O = 1 V_{pp}, R_L = 2 kΩ, A_V = +1, f = 10 kHz		–	0.025	–	
Power Supply						
Power Supply Rejection Ratio		PSRR	80	100	–	dB
Quiescent Current	No load, per channel	I_{DD}	–	275	575	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

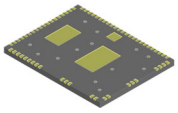
5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.
7. The minimum width of the input pulse should exceed 500 ns to ensure the filtering time of the input filter is exceeded.
8. MDT is defined as |DT1−DT2| referenced to 0.
9. MT is defined as an absolute value of matching delay time between High−side and Low−side.
10. PM is defined as an absolute value of matching pulse−width between Input and Output.

ORDERING INFORMATION

Device	Package	Shipping†
NFMECS640A0	WQFN65 13 × 10, 0.5P (Pb−Free)	3000 / Tape & Reel

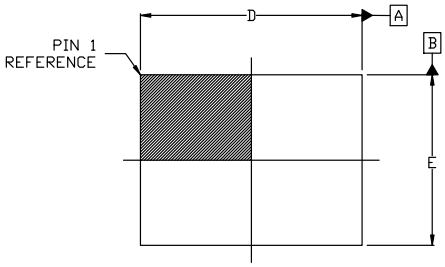
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

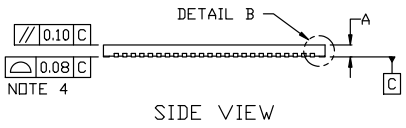
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

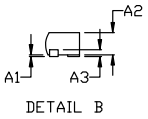


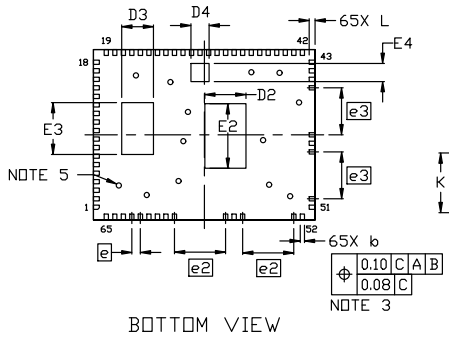
GAQFN65 13x10, 0.5P
CASE 510CT
ISSUE C

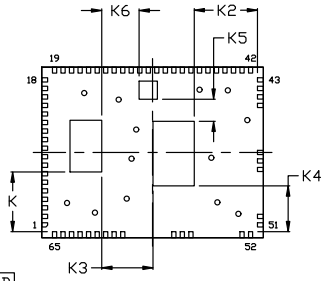
DATE 14 DEC 2021







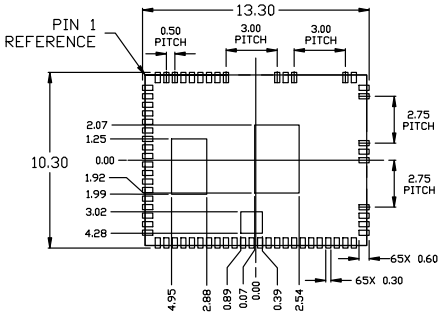




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. 13X MOLD POST AT BOTTOM OF PACKAGE Ø0.3mm REF.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A2	0.65 REF		
A3	0.10 REF		
b	0.20	0.25	0.30
D	12.90	13.00	13.10
D2	2.31	2.41	2.51
D3	1.76	1.86	1.96
D4	0.98	1.08	1.18
E	9.90	10.00	10.10
E2	3.69	3.79	3.89
E3	2.94	3.04	3.14

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	0.96	1.06	1.16
e	0.50 BSC		
e2	3.00 BSC		
e3	2.75 BSC		
K	3.50 REF		
K2	3.72 REF		
K3	3.00 REF		
K4	2.68 REF		
K5	1.30 REF		
K6	2.20 REF		
L	0.25	0.35	0.45



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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PUBLICATION ORDERING INFORMATION

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